

# Neuron Microchips

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## Abstract

A novel microchip implementation for an associative neuron group is presented. This microchip is intended for human-like cognitive systems where information is processed via links between distributed representation signal arrays. In this study a microchip containing 8 associative neurons and 128 synaptic connections was realized by 0.35  $\mu\text{m}$  CMOS process. The synaptic weights have been implemented using an analog nonvolatile EEPROM's. Measurements show that the presented ideas work and the neuron group is able to associate signal arrays together as intended.

## 1. Introduction

Processing with distributed signal representations calls for the ability to associate representations to each other so that one representation can be evoked by another. Distributed signal representations consist of arrays of individual signals, therefore processing with them reduces into operations with individual signals. Thus a basic signal processing unit able to associate individual signals is needed. A simple artificial associative neuron is a circuit element that is able to learn the association between two signals, namely a main signal and an associative signal. After learning the associative signal alone shall be able to evoke the main signal. This kind of an associative mechanism is also known as Hebbian learning. This kind of a neuron can be realized quite simply. We need a "synapse", a synaptic switch that becomes permanently closed when learning takes place, i.e. when the main signal and the associative signal appear simultaneously. A closed synaptic switch will then allow the evocation of the main signal by the associative signal.

## 2. Associative microchip

We have studied a number of neuron microchips for different applications, like neuron decoders [1] and AD and DA converters [2]. These have been based on floating gate CMOS (FGCMOS) that is sometimes also called neuron CMOS [3]. This paper presents neurochips based on the associative architecture proposed by P. Haikonen [4,5]. A novel neuron group has been investigated. Technical properties have been published earlier [6,7]. An associate neuron group microchip was designed by using ideas described in [4,5].

Following specifications were set for the neuron group:

- A synapse matrix with 8 rows and 16 columns
- 16 associative inputs (a) and 8 signal inputs (s)
- 8 neurons each connected top the synapse row of 16 synapses, 8 signal outputs (so)
- Maximal flexibility for chip biasing and control (external controls preferred)

The flexibility of the microchip is essential, since it was designed to suit several different neuron group applications. Thus, the biasing of the voltage buffers and comparators can be altered afterwards to make compromises between the speed and power consumption. A simplified schematic of the associate microchip is shown in Fig. 1. Only the main blocks and global wiring are shown in order to keep the schematic more readable.

### 2.1 Neuron

The function of the neurons is to combine information of each synapse row and compose corresponding output signals. The neurons also generate required threshold-signals and winner-takes-all functionality. The details of the used neuron topology are described in detail in paper published earlier [6].

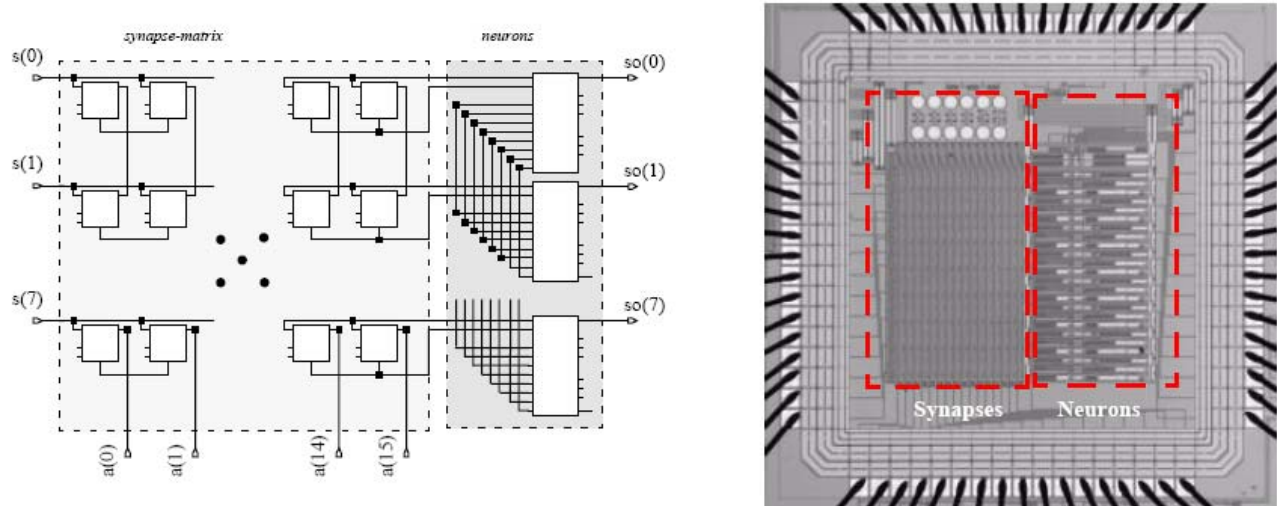


Figure 1. A simplified schematic of the associative microchip and the photograph of the chip ( $1.3 \times 1.2 \text{ mm}^2$ ).

## 2.2 Synapse

A synaptic connection is established between signals during a learning period, when the incoming main signal  $s$  and associative signal  $a$  appear simultaneously. In many cases instant learning is not preferred as the association might be formed by a random coincidence. Therefore the synapse must be modified to include a temporal filter, for instance a leaky accumulator and a threshold circuit. The implementation large number of synaptic weights using digital logic has several drawbacks: large silicon area, a fixed number of states needed to make an association and volatile operation. In order to overcome these problems a custom analog nonvolatile memory was designed for the synaptic weight connections within this study. Following guidelines were set for required synaptic weight or memory cell:

- a) compatible with a standard CMOS, b) nonvolatile, c) a 'linear' response to program, d) minimal program voltages and currents, e) compatibility to proposed synapse topology, and f) reliability.

## 3. Realisation

An associative neuron group microchip was laid out using standard  $0.35 \mu\text{m}$  CMOS process provided by AMS Micro Systeme and active area measures  $1.3 \times 1.2 \text{ mm}^2$  silicon area. A photograph of the chip is shown in Fig. 2.

## 4. Conclusion

A microchip containing 8 associative neurons and 128 synaptic connections was realized. The synaptic weights have been implemented using analog nonvolatile EEPROM's. Measurements show that the presented ideas work and the neuron group is able to associate signal arrays together as intended and the proposed analog EEPROM structure is operating accurately and it can be programmed in a reliable manner using a standard CMOS technology.

## References

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